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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,019	10/05/2001	Myles H. Wakayama	47426/RJP/B600	3152

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EXAMINER
KINKEAD, ARNOLD M

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 05 12 2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,019	WAKAYAMA, MYLES H.	
	Examiner	Art Unit	
	Arnold M Kinkead	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 24-32, and 34-45 rejected under 35 U.S.C. 102(b) as being anticipated by Gersbach et al.

The reference by Gersbach et al discloses a CMOS charge pump that is part of a PLL loop(see figures 1 and 2). Figure 1 shows the PLL with detector(12) receiving input data, charge pump(14), and timing reference generator(18). In figure 2, first(H4) and second primary(H12) current sources are shown. The Gersbach et al reference meets the broad recitation for parallel current paths, the first path includes H4(first current source at first end), T2,T3,T7(second source at second end) the second path including H12(first current source),T1,T6 T8(second current source) and they have the same configuration(i.e. parallel) with corresponding feedback. The first output node for the first path include the point between H4,H17 which is also coupled to RC filter(on node 31); the output node for the second path is coupled between H12,H3 which is also coupled to node 31. A first output node(31) and second output node(49) are shown. A filter(RC in general) is coupled to the first node and a LOOP capacitor C is shown in figure 4. A first output node(31) and second output node(49) are shown. A filter(RC in general) is coupled to the first node and a LOOP capacitor C is shown in figure 4. A feedback path is shown connected to reduce DC offset(note in col. 1, lines 48-60, The CMOS or transistors are part of the problem due to the channel length modulation, i.e. parasitics, that lead to the

offset) at charge pump output. The adjustment current being developed by way of T4,T5. The method steps being inherent.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gersbach et al(US 5,508,660 cited by applicant).

The reference by Gersbach et al discloses a CMOS charge pump that is part of a PLL loop(see figures 1 and 2). Figure 1 shows the PLL with detector(12) receiving input data, charge pump(14), and timing reference generator(18). In figure 2, first(H4) and second primary(H12) current sources are shown. The Gersbach et al reference meets the broad recitation for parallel current paths, the first path includes H4(first current source), T2,T3,T7(second current

source) the second path including H12(first current source),T1,T6,T8(second current source) and they have the same configuration(i.e. parallel) with corresponding feedback. The first output node for the first path include the point between H4,H17 which is also coupled to RC filter(on node 31); the output node for the second path is coupled between H12,H3 which is also coupled to node 31. A first output node(31) and second output node(49) are shown. A filter(RC in general) is coupled to the first node and a LOOP capacitor C is shown in figure 4. A feedback path is shown connected to reduce DC offset (note in col. 1, lines 48-60, The CMOS or transistors are part of the problem due to the channel length modulation, i.e. parasitics, that lead to the offset) at charge pump output. The adjustment current being developed by way of T4,T5.

The reference does not describe a particular RC filter configuration, however, a series RC in parallel with another resistor. This , however, is a conventional circuit used as a low pass filter for developing the VCO control signal, notoriously well known to one of ordinary skill in the art.

In light of the above it would have been obvious to one of ordinary skill in the art to have recognized that the general low pass filter of the reference may be one of several notoriously well known configurations to allow for the control signal to be developed for the VCO as is conventional and well within the level of skill for one of ordinary skill in the art.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claim 45 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of U.S. Patent No. 6,181,210. Although the conflicting claims are not identical, they are not patentably distinct from each other because the application(09/972,019) claim 45 claims a method of controlling a charge pump with two parallel current paths formed of transistors each path having an output node coupled between a first and second current sources...operating within a PLL comprising the steps of detecting a phase/frequency characteristic...to produce an output signal, receiving said output signal at said charge pump..to produce a pump control signal, and generating a characteristic current using one of said first or second current paths and controlling a value of one of said current sources to minimized DC offset resulting from parasitic capacitance of the transistors.

This claim is merely a broad presentation of what has been claimed in the apparatus claim 1 of the patent(US 6,181,210)

The patent claim 45 meets most of the elements that operate to meet the steps as described above, including the PLL charge pump, a phase frequency detector, a charge pump with two parallel paths coupled between pump-up and pump down current sources. A characteristic current is developed by source or sing current sources, and feedback means used for controlling(balancing) the current sources to minimize DC offset.

The patent does not claim the DC offset resulting from parasitics of the transistors but one of ordinary skill in the art would have recognized that the DC offset in the charge pump as claimed in the patent does inlclude parasitic

capacitances that are part of all transistors and notoriously well known in the art to lead to offsets and misalignment if proper matching of the components are not met. This leads to frequency instability of the PLL.

In light of the above it would have been obvious for one of ordinary skill in the art to have recognized that the patent claim meets the broad method steps for a PLL with charge pump operation and DC offset including parasitics of transistors used within the charge pump; this being a well documented problem in the prior art with regards improving frequency stability for PLL applications.

7. Claim 45 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of U.S. Patent No. 6,326,852. Although the conflicting claims are not identical, they are not patentably distinct from each other because the application(09/972,019) claim 45 claims a method of controlling a charge pump with two parallel current paths formed of transistors each path having an output node coupled between a first and second current sources...operating within a PLL comprising the steps of detecting a phase/frequency characteristic...to produce an output signal, receiving said output signal at said charge pump..to produce a pump control signal, and generating a characteristic current using one of said first or second current paths and controlling a value of one of said current sources to minimized DC offset resulting from parasitic capacitance of the transistors.

This claim is merely a broad presentation of what has been claimed in the apparatus claims 1 and 2 of the patent(US 6,326,852)

The patent claim 45 meets most of the elements that operate to meet the steps as described above, including the PLL charge pump, a phase frequency detector, a charge pump with two parallel paths coupled between pump-up and

pump down current sources. A characteristic current is developed by source or sing current sources, and feedback means used for controlling(balancing) the current sources to minimize DC offset.

The patent does not claim the DC offset resulting from parasitics of the transistors but one of ordinary skill in the art would have recognized that the DC offset in the charge pump as claimed in the patent does inlclude parasitic capacitances that are part of all transistors and notoriously well known in the art to lead to offsets and misalignment if proper matching of the components are not met. This leads to frequency instability of the PLL.

In light of the above it would have been obvious for one of ordinary skill in the art to have recognized that the patent claim meets the broad method steps for a PLL with charge pump operation and DC offset including parasitics of transistors used within the charge pump; this being a well documented problem in the prior art with regards improving frequency stability for PLL applications.

Response to Arguments

8. Applicant's arguments filed 02-27-03 have been fully considered but they are not persuasive. The examiner has considered applicant' s remarks about the first and second current paths having respective first and second output nodes with a filter coupled to said first output node and a capacitor coupled to the second output node.. The Gersbach et al reference meets the broad recitation because it too has parallel current paths, the first path includes H4, T2,T3, T7the second path including H12,T1,T6,T8 and they have the same configuration(i.e. parallel) with corresponding feedback. The first output node for the first path include the point between H4,H17 which is also coupled to RC filter(on node 31); the output node for the second path is coupled between H12,H3 which is also coupled to node 31.

With regards the capacitor, figure 4 shows such a capacitor coupled to second output nodes of T17,T14 each transistor has a separate output tied to the capacitor. (note in col. 1, lines 48-60, The CMOS technology or transistors are part of the problem due to the channel length modulation, i.e. parasitics, that lead to the offset)

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M Kinkead whose telephone number is 703-305-3486. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner' s supervisor, Robert Pascal can be reached on 703-308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Arnold M Kinkead
Primary Examiner
Art Unit 2817

Arnold Kinkead
May 7, 2003